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| **stack Project Status** | | | |
| **Project File:** | stackk.xise | **Parser Errors:** | No Errors |
| **Module Name:** | stack | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc3s500e-4ft256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | [2 Warnings (2 new)](D://23bec15556/stackk/_xmsgs/*.xmsgs?&DataKey=Warning) |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://23bec15556/stackk/stack.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** | [All Constraints Met](D://23bec15556/stackk/stack.ptwx?&DataKey=ConstraintsData) |
| **Environment:** | [System Settings](D://23bec15556/stackk/stack_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://23bec15556/stackk/stack.twx?&DataKey=XmlTimingReport) |

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| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Flip Flops | 17 | 9,312 | 1% |  | |
| Number of 4 input LUTs | 178 | 9,312 | 1% |  | |
| Number of occupied Slices | 94 | 4,656 | 2% |  | |
| Number of Slices containing only related logic | 94 | 94 | 100% |  | |
| Number of Slices containing unrelated logic | 0 | 94 | 0% |  | |
| Total Number of 4 input LUTs | 185 | 9,312 | 1% |  | |
| Number used as logic | 50 |  |  |  | |
| Number used as a route-thru | 7 |  |  |  | |
| Number used for 32x1 RAMs | 128 |  |  |  | |
| Number of bonded [IOBs](D://23bec15556/stackk/stack_map.xrpt?&DataKey=IOBProperties) | 21 | 190 | 11% |  | |
| Number of BUFGMUXs | 1 | 24 | 4% |  | |
| Average Fanout of Non-Clock Nets | 7.08 |  |  |  | |

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| **Performance Summary** | | | | [**[-]**](?&ExpandedTable=PerformanceSummary) |
| **Final Timing Score:** | 0 (Setup: 0, Hold: 0) | **Pinout Data:** | [Pinout Report](D://23bec15556/stackk/stack_par.xrpt?&DataKey=PinoutData) | |
| **Routing Results:** | [All Signals Completely Routed](D://23bec15556/stackk/stack.unroutes) | **Clock Data:** | [Clock Report](D://23bec15556/stackk/stack_par.xrpt?&DataKey=ClocksData) | |
| **Timing Constraints:** | [All Constraints Met](D://23bec15556/stackk/stack.ptwx?&DataKey=ConstraintsData) |  |  | |

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| **Detailed Reports** | | | | | | [**[-]**](?&ExpandedTable=DetailedReports) |
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** | |
| [Synthesis Report](D://23bec15556/stackk/stack.syr) | Current | Mon 8. Sep 16:11:19 2025 | 0 | [2 Warnings (2 new)](D://23bec15556/stackk/_xmsgs/xst.xmsgs?&DataKey=Warning) | [2 Infos (2 new)](D://23bec15556/stackk/_xmsgs/xst.xmsgs?&DataKey=Info) | |
| [Translation Report](D://23bec15556/stackk/stack.bld) | Current | Mon 8. Sep 16:17:13 2025 | 0 | 0 | 0 | |
| [Map Report](D://23bec15556/stackk/stack_map.mrp) | Current | Mon 8. Sep 16:17:19 2025 | 0 | 0 | [2 Infos (2 new)](D://23bec15556/stackk/_xmsgs/map.xmsgs?&DataKey=Info) | |
| [Place and Route Report](D://23bec15556/stackk/stack.par) | Current | Mon 8. Sep 16:18:15 2025 | 0 | 0 | [2 Infos (2 new)](D://23bec15556/stackk/_xmsgs/par.xmsgs?&DataKey=Info) | |
| Power Report |  |  |  |  |  | |
| [Post-PAR Static Timing Report](D://23bec15556/stackk/stack.twr) | Current | Mon 8. Sep 16:18:18 2025 | 0 | 0 | [6 Infos (6 new)](D://23bec15556/stackk/_xmsgs/trce.xmsgs?&DataKey=Info) | |
| [Bitgen Report](D://23bec15556/stackk/stack.bgn) | Current | Mon 8. Sep 16:18:31 2025 | 0 | 0 | 0 | |

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| **Secondary Reports** | | | [**[-]**](?&ExpandedTable=SecondaryReports) |
| **Report Name** | **Status** | **Generated** | |
| [WebTalk Report](D://23bec15556/stackk/usage_statistics_webtalk.html) | Current | Mon 8. Sep 16:18:32 2025 | |
| [WebTalk Log File](D://23bec15556/stackk/webtalk.log) | Current | Mon 8. Sep 16:18:33 2025 | |

**Date Generated:** 09/15/2025 - 15:06:40